This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-15 (canceled)

Claim 16 (currently amended): ~~The~~ A semiconductor integrated circuit ~~according to claim 1,~~ having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising:

a plurality of first capacitors that are charged during a first period;

a plurality of second capacitors provided alternately with the first capacitors, the second capacitors being charged during a second period;

a first potential converter for supplying a boosted clock to each first capacitor;

a second potential converter for supplying a boosted clock to each second capacitor;

a first transfer device for transferring charges stored in each first capacitor to the succeeding second capacitor during a third period that is delayed from the second period by a predetermined time; and

a second transfer device for transferring charges stored in each second capacitor to the succeeding first capacitor during a fourth period that is delayed from the first period by a predetermined time,

wherein the first potential converter includes:

a third capacitor, a first terminal thereof being connected to a high-level side power terminal via a first switching device, a second terminal thereof being connected to a low-level side power terminal via a second switching device that is turned on simultaneously with the first switching device;

a third switching device that is turned on in opposite timing for the first and the second switching devices to supply a driving potential to the second terminal of the third capacitor;

a fourth switching device that is turned on simultaneously with the third switching device to connect the first terminal of the third capacitor to an output terminal; and

a fifth switching device that is turned on simultaneously with the first switching device to reset a potential at the output terminal,

wherein the third capacitor is charged while the first and the second switching devices are on and the charged third capacitor is coupled to the first capacitor in series while the third and the fourth switching devices are on.

Claims 17-18 (canceled)

Claim 19 (previously presented): The semiconductor integrated circuit according to claim 16, wherein the third period terminates by a predetermined time before the succeeding second period starts.

Claim 20 (previously presented): The semiconductor integrated circuit according to claim 16, wherein the fourth period terminates by a predetermined time before the succeeding first period starts.

Claim 21 (currently amended): ~~The~~ A semiconductor integrated circuit ~~according to claim 1,~~ having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising:

a plurality of first capacitors that are charged during a first period;

a plurality of second capacitors provided alternately with the first capacitors, the second capacitors being charged during a second period;

a first potential converter for supplying a boosted clock to each first capacitor;

a second potential converter for supplying a boosted clock to each second capacitor;

a first transfer device for transferring charges stored in each first capacitor to the succeeding second capacitor during a third period that is delayed from the second period by a predetermined time; and

a second transfer device for transferring charges stored in each second capacitor to the succeeding first capacitor during a fourth period that is delayed from the first period by a predetermined time,

wherein the second potential converters includes:

a third capacitor, a first terminal thereof being connected to a high-level side power terminal via a first switching device, a second terminal thereof being connected to a low-level side power terminal via a second switching device that is turned on simultaneously with the first switching device;

a third switching device that is turned on in opposite timing for the first and the second switching devices to supply a driving potential to the second terminal of the third capacitor;

a fourth switching device that is turned on simultaneously with the third switching device to connect the first terminal of the third capacitor to an output terminal; and

a fifth switch device that is turned on simultaneously with the first switching device to reset a potential at the output terminal,

wherein the third capacitor is charged while the first and the second switching devices are on and the charged third capacitor is coupled to the first capacitor in series while the third and the fourth switching devices are on.

Claims 22-23 (canceled)

Claim 24 (previously presented): The semiconductor integrated circuit according to claim 21, wherein the third period terminates by a predetermined time before the succeeding second period starts.

Claim 25 (previously presented): The semiconductor integrated circuit according to claim 21, wherein the fourth period terminates by a predetermined time before the succeeding first period starts.